PowerDRC/LVS
Release Notes

Last update: Jan, 2021
Product version: 2.7

New in this version

- Improved extraction of custom device parameters and comparison

- Improved control over parameters comparison

- Improved merging of parallel devices in NVN

- Improved diagnostics in parameters matching

- Improved scaling of parameters for custom devices

- Improved calculation of M-parameter inside a custom **subckt**

- Added support of **CentOS 7.9**

- Added RCF parameters:

  - **CheckInternalNetsForCellMerge** to speed up sorting of parallel cells and their merging

  - **ExtractionPropertiesParametersOnly** to suppress calculation of standard parameters of built-in devices

  - **ParasiticExtractionResToIgnore** to explicitly list models to be interpreted as parasitic resistances

  - **NoParameterArgumentsSwap** to control swap of arguments in **perimeter_inside** and **perimeter_outside**

  - **NetParameterDump** to control generation of antenna ratio report

Known issues

- During XOR operation, discrepancies of certain types on strip margins may be presented by two shapes in multi-CPU mode instead of one shape in single-CPU mode resulting in different total number of discrepancies reported in summary.

- There may be problems when processing large designs on 32-bit platforms, in particular:

  - XOR operation may run out of memory
  - Short Finder may run out of memory
  - Extraction may stop with a message about too many files open

  The issues do not manifest on 64-bit platforms.

- In this version of **PowerDRC/LVS** hierarchical fills are not available in **native OpenAccess** format

- There may be a notable slowdown when processing big net lists with **MergeSplitGates** option switched ON. We recommend to turn the option off in such cases.

- Sometimes **PowerDRC/LVS** can be slowed down by anti-virus software installed on **Windows** machine. You may want to add an exception for run directory in your anti-virus software, so that files in the run directory are not checked for viruses.

- Sometimes when opening **DRC Results** window, **PowerRDE** loads results of the second to last run instead of the latest results. Click **Reload** to update run results.

- In this version of **PowerDRC/LVS**, when working in the hierarchical mode of DRC/LVS in **Cadence Virtuoso**, user has to manually bring an active **Virtuoso** window to the front due to a known issue in **Cadence** API.

- When **PowerDRC/LVS** is running on **Windows** platform the number of characters in a path or a name that is specified as variable value in DRC RCF or NVN RCF cannot be greater than 255.

- Sometimes LVS operation may stop on comparison stage with message "PowerLVS has exited with code 111". If that is the case:
  - Please pay attention to case sensitivity, especially under Linux OS and check all settings
  - Double check your settings of **CaseIgnore** parameter
  - If you see different cell names for schematic and layout please use a bind file to specify corresponding pairs.

- In this version of **PowerDRC/LVS**, **PowerRDE** doesn't support definition of multiple layout files for Merge option of fill layers generation.

- On large layouts with flat netlists, using "**MergeSplitGates : yes**;" in RCF when labels are absent or not good may cause severe slowdown and high memory consumption. To workaround the issue turn the option off with "**MergeSplitGates : no**;".

- Files in **Laker** format aren't supported by XOR mode

- Sometimes, on Windows machine, you may get "Cannot find license file" message with -1,359 error code despite of the valid path to the file. That may be caused by Data Execution Prevention in Windows. To remedy the problem, try the following steps:

    - Stop your License Server
    - Start the Data Execution Protection from Control Panel > System > Advanced > Performance Settings > Data Execution Prevention.
    - Either stop Data Execution Protection or add exceptions for Lmgrd.exe
    - Restart the License Manager